TSC701
the SPARC Communication Controller
# that breaks the limits of your Application

The TSC701 is a **32-bit Embedded SPARC Processor** especially designed for the Communication Market. Built around TEMIC's **SPARClet™ architecture**, the TSC701 provides a full one-chip system solution with a high performance core integrating **DSP and High Speed HDLC Controllers** and the necessary peripherals for this field of application.

Performance

- **50 MIPS** (@50MHz) SPARC V8 Compatible CPU
- High HDLC Processing Power: from **96** full duplex channels (worst case) up to **336 channels** (best case configuration).
- Up to **8 Mbps** Transmission Speed on each of the **4 HSSL** (High Speed Serial Line).
- **DSP** capability: one cycle efficient 32x32-bit multiplier.

Key Features

- Communications Functions:
  - Communication Coprocessor (CCP)
  - 4 HSSL: asynchronous, synchronous (Point to Point and Multipoint) and PCM (T1, E1, T2... lines)
- DSP Capability:
  - Fully Parallel On-Chip 32x32-bit Multiplier
- Integrated Instruction Cache (16 KB) and Data Cache (8 KB)
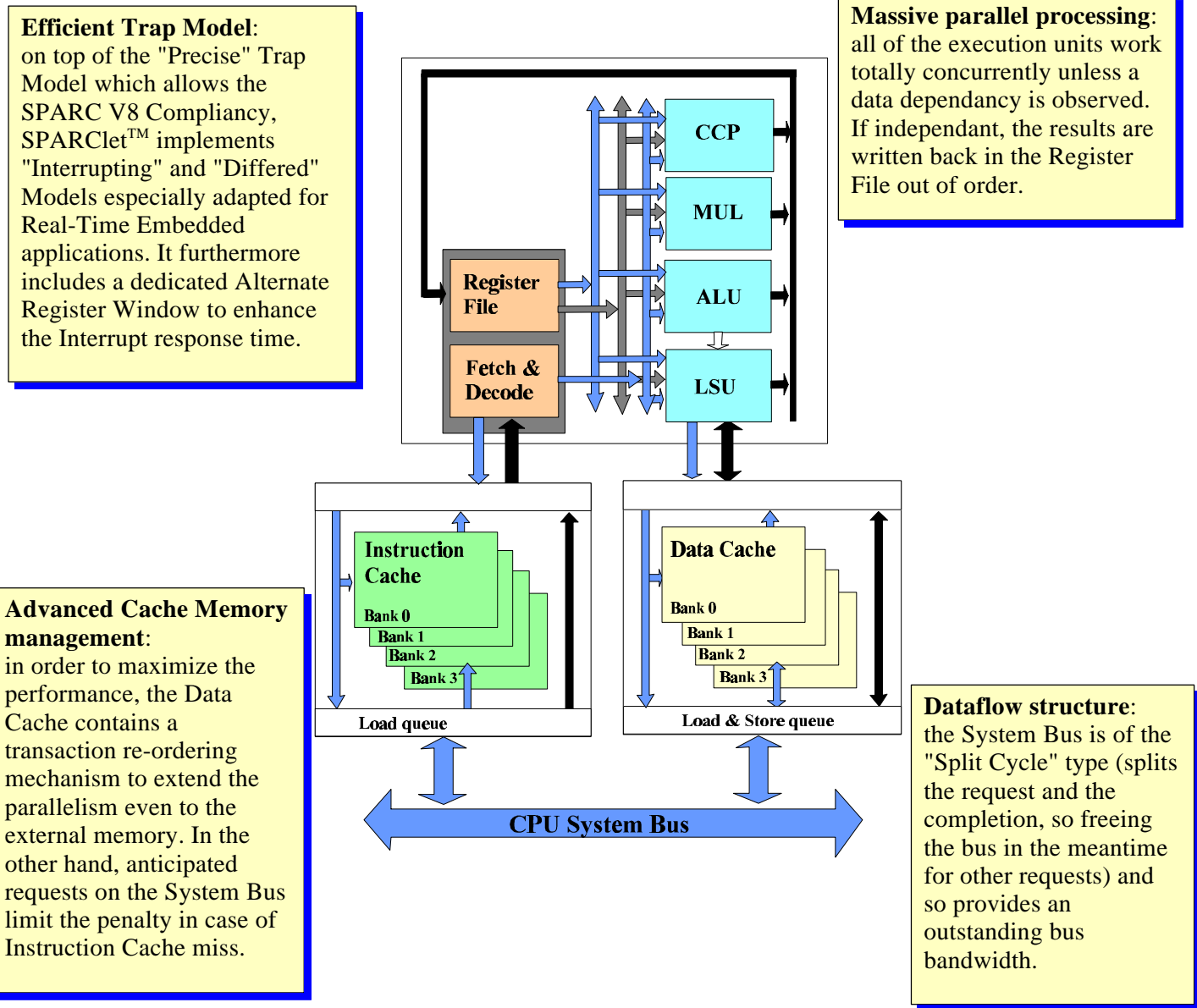- Multiprocessing Capability.
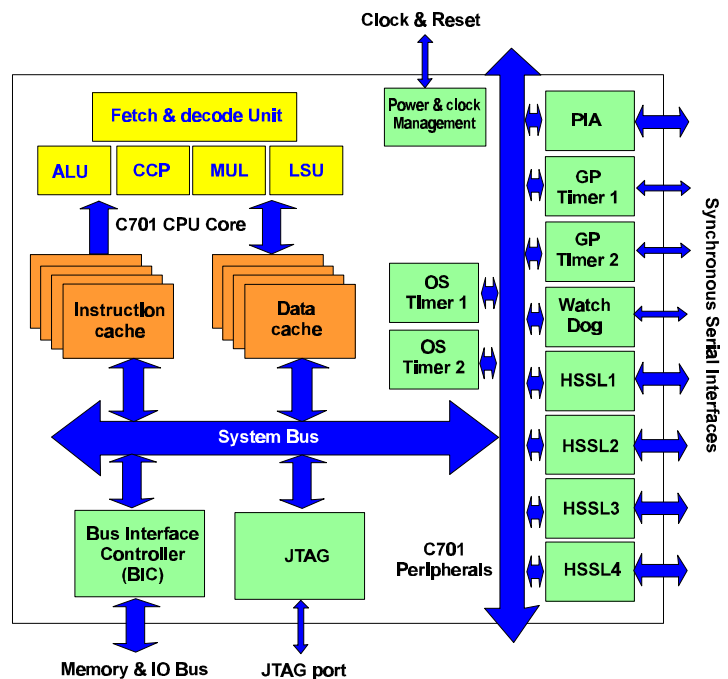
Typical Applications	Main Benefits
• Cellular Phone Base Stations	• Integration of the DSP function • Multiprocessing
• ISDN Routers	• Meet today's and tomorrow's bit rates requirements
• WAN Switching systems	• Up to 336 HDLC channels

TEMIC
Semiconductors

About the SPARClet™ Architecture

SPARClet™ Architecture has been developed by TEMIC and especially designed for the Embedded Market. Beside being fully SPARC V8 Compliant and so benefiting of the Tools running on Sun SPARCstations, SPARClet™ provides extra features in the areas of real-time performance and on-chip DSP functions.

SPARClet™ is based upon the following principles:

Efficient Trap Model:
on top of the "Precise" Trap Model which allows the SPARC V8 Compliancy, SPARClet™ implements "Interrupting" and "Differed" Models especially adapted for Real-Time Embedded applications. It furthermore includes a dedicated Alternate Register Window to enhance the Interrupt response time.

Massive parallel processing:
all of the execution units work totally concurrently unless a data dependancy is observed. If independant, the results are written back in the Register File out of order.

Advanced Cache Memory management:
in order to maximize the performance, the Data Cache contains a transaction re-ordering mechanism to extend the parallelism even to the external memory. In the other hand, anticipated requests on the System Bus limit the penalty in case of Instruction Cache miss.

Dataflow structure:
the System Bus is of the "Split Cycle" type (splits the request and the completion, so freeing the bus in the meantime for other requests) and so provides an outstanding bus bandwidth.

The SPARC V8 Instruction Set has been enriched with new instructions: SCAN (bit scanning), Shuffle (bit/nibble/byte/half-word swapping), and the instructions dedicated to the on-chip coprocessors (MUL and CCP for the TSC701).

Design your application around the TSC701

In order to provide a comprehensive solution, a full range of software and debug tools has been developed around the TSC701.

Code Development Tools

Although SPARClet™ is binary compatible with the widely spread SPARC V8 standard and as so can use any available compliant compiler, an optimized compiler is needed to take the architecture best benefits (parallel processing) and to use the additional instructions (SCAN, SHUFFLE and the specific internal co-processors instruction set).

The California based company CYGNUS, one of the compiler's market leaders, provides the SPARClet™ CDK (CYGNUS Development Kit) package which includes a GNU based C/C++ compiler and the RGDB remote debugger.

The CDK environment package is proposed for Sun OS, Solaris and Windows 3.1 platforms.
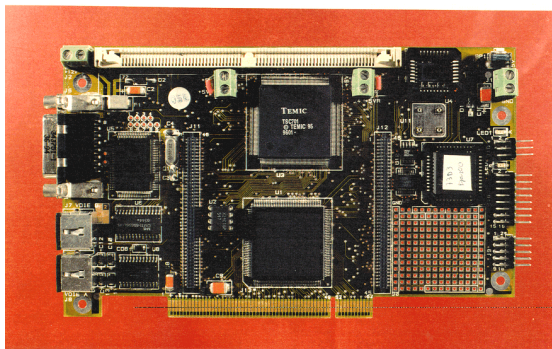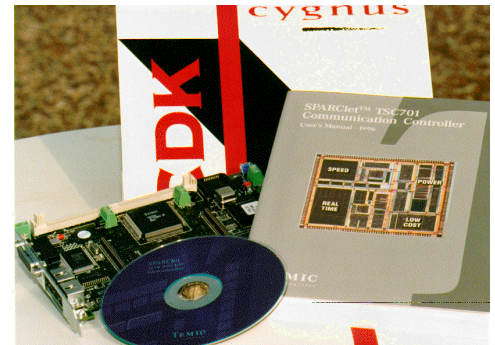
Starter & Application Kits

Those support kits available from TEMIC include:
- the TSC701 Demonstration Board (PCI, Ethernet)
- a debug monitor
- the necessary software libraries for:
  - the on-chip peripherals and coprocessors
  - the basic applicative functions (HDLC, Software DMA,...)
- the SPARClet™ CDK

Real-Time Operating System

The two first Operating Systems ported to the SPARClet™ architecture are:
- Chorus OS from Chorus Systems
- VxWorks/Tornado from Wind River Systems
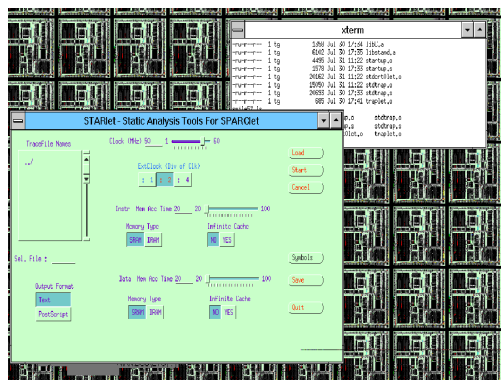
Development and Debug Tools

Architecture Simulator
The SASlet package provides an easy way to simulate and debug TSC701 code and to evaluate its performance prior to the availability of the hardware target.

Logic analyser
SPARClet™ dedicated tools including hardware probes and on-line disassembling are developed by Tektronics.

ROM emulator
TEMIC recommends XLNT ROM emulation equipments.

JTAG tool
Will be available early 1997.

Real-Time Trace and Performance monitoring
TEMIC recommends CodeTest from AMC

TSC701 Features

CPU Core

- V8 compliant SPARC Processor
  - Little & Big Endian data organizations supported
  - Multiply and Accumulate instructions
  - Bit scanning and bit shuffling instructions
  - 8 Register Windows (**136 registers**)
  - Alternate Window Registers (**32 registers**)
  - Communication Coprocessor (CCP)
    Coder/Decoder/CRC
    Supported protocols: HDLC,V.110, proprietary
    100 Mbps max. @ 50MHz
- On-Chip Cache Memory
  - Four ways associative
  - Lockable by Bank
  - Instruction Cache: **16 KBytes**
  - Data Cache: **8 KBytes**
- System Bus
  Split Cycle Bus connecting the Core and the On-Chip Peripherals
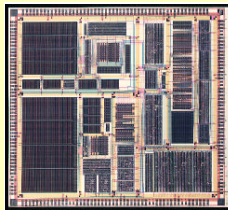
On-Chip Peripherals

- Bus Interface Controller (BIC)
  - 256 Mbytes address space
  - **DRAM / SRAM / ROM** glueless interface
  - Programmable Timings
  - **Multimaster bus** support
  - 8–bit boot feature
  - Control signals generated for 48 Mbytes.
- JTAG Test Access Port
  - Boundary Scan
  - System Bus agents access for debug purpose
- Peripheral Interface Adapter (PIA)
  - 10–bit bi-directional port
  - **Programmable Interrupt Level**
- Serial Links
  - 4 High Speed Serial Links (HSSL)
  - support of asynchronous, synchronous (Point to Point and Multipoint) and PCM
- Timers
  - 2 General Purpose Timers
  - 2 Operating System Timers
  - 1 Watchdog

Technology

- Fully static CMOS Technology
- Temperature Range: 0 to 70°C
- Operating Frequency: 33MHz & 50MHz
- Packages: 225-pin BGA, 208–pin PQFP and 209–pin PGA

On-line support

- SPARClet™ e-mail hot-line: sparclet@temic.fr
- ftp site: public.matramhs.fr
  (directory: /pub/pbomel-dad)
- WWW
  TEMIC: www.temic.de
  CYGNUS: www.cygnus.com
  Chorus Systems: www.chorus.com
  Wind River Systems: www.wrs.com
  SPARC International: www.sparc.com

Available Documentation

- TSC701 User's Manual
- TSC701 Electrical & Mechanical Specification
- TSC701 Starter-Kit User's Guide
- SPARClet™ Brochure
- SPARClet™ CD ROM